Exhibit 9

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By Sherry Barton

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sze-Ki Mo, et al. Application No.: 08/970,221 Filed: November 17, 1997 For: FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE	Examiner: Unassigned Art Unit: 1107 PRELIMINARY AMENDMENT

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants respectfully request that the following amendments and remarks be entered prior to examination of the above-identified CPA.

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IN THE CLAIMS:

Please cancel claim 13, amend claims 1, 6-8, 10, 18, 47 and 50-51 and add new claims 53-55 as set forth below. For convenient reference, all pending claims are reproduced below with unamended claims appearing in smaller font.

Sub D1

C1

1. (Twice Amended) A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

Cont'd C1

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein[,] the heavy body forms an abrupt junction with the well and the depth of **[said doped heavy body]** the junction, relative to the depth of the well, is controlled so that **[the peak electric field]** a transistor breakdown initiation point **[, when voltage is applied to the transistor, will be]** is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

5. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

C2

4 ~~6~~. (Once Amended) The trenched field effect transistor of claim 1 wherein **[there is an]** the abrupt junction **[at the interface between the heavy body and the well, to cause]** causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor **[to occur in the area of the interface]**.

5 ~~7~~. (Twice Amended) The trenched field effect transistor of claim 4 ~~6~~ wherein said doped heavy body has a first dopant concentration near the **[doped heavy body interface,]** abrupt junction and a second dopant concentration near its upper surface that is less than the first dopant concentration **[near its upper surface]**.

Sub B3

8. (Twice Amended) An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, **[and]** each trench extending a predetermined depth into said substrate and **[in a first**

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direction,] the space between adjacent trenches defining a contact area[**, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches**];

[surrounding each trench,] a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well ~~having a second conductivity type~~ with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

Cont'd C2

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area[.],
wherein the heavy body forms an abrupt junction with the junction, relative to a depth of the well, is controlled so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

9. The array of transistor cells of claim 8, wherein each said doped well has a substantially flat bottom.

C3

8 ~~10~~. (Once Amended) The array of transistor cells of claim 6 ~~8~~ wherein [the depth of each heavy body region relative to the depths of the wells and the gate-forming trenches is selected so that the peak electric field when voltage is applied to the transistor will] the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.

11. The array of transistor cells of claim 8 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.

12. The array of transistor cells of claim 8 wherein each said gate-forming trench has rounded top and bottom corners.

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13. (Canceled)

14. (Once Amended) The array of transistor cells of claim 8 further comprising a field termination structure surrounding the periphery of the array.

15. The array of transistor cells of claim 14 wherein said field termination structure comprises a well having a depth greater than that of the gate-forming trenches.

16. The array of transistor cells of claim 14 wherein said field termination structure comprises a termination trench extending continuously around the periphery of the array.

17. The array of transistor cells of claim 16 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

C4

18. (Twice Amended) A semiconductor die comprising:

a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate having a first conductivity type, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same;

a doped well having a second conductivity type of a charge opposite that of the first conductivity type, said doped well formed in the semiconductor substrate between each pair of gate-forming trenches within which source junctions having the first conductivity type are formed, said doped well extending to a depth that is less than said predetermined depth of said gate-forming trench; **[and]**

a doped heavy body having the second conductivity type positioned between source junctions in the doped well; and

[surrounding the periphery of the array,] a field termination structure in contact with the heavy body, surrounding the periphery of the array, and **[that]** extend**[s]**ing into the semiconductor substrate to a depth that is deeper than said depth of said **[doped]** well.

19. (Once Amended) The semiconductor die of claim 18 wherein said field termination structure comprises a deep doped well.

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20. The semiconductor die of claim 18 wherein said field termination structure comprises a termination trench.

21. The semiconductor die of claim 20 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

22. *(Once Amended)* The semiconductor die of claim 18 wherein each of said DMOS transistor cells further comprises a doped heavy body extending into said doped well to a depth that is less than the depth of said doped well.

46. The array of transistor cells of claim 8 wherein the doped heavy body forms a continuous doped region along substantially the entire length of said contact area.

sub D3

47. (Once Amended) A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

C5

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth[;],

wherein[,] the doped heavy body,

forms a continuous doped region along substantially the entire longitudinal axis of a trench[.], and

forms an abrupt junction with the well and depth of the junction, relative to a maximum depth of the well, is controlled so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

48. The trenched field effect transistor of claim 47 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.

49. The trenched field effect transistor of claim 48 wherein the contact areas alternate between source and heavy body contacts.

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C6

50. (Once Amended) The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well,

wherein[,] the **[controlled]** the relative depths of the doped heavy body and the well are controlled to eliminate[s] the need for any **[additional epitaxial]** layers disposed between the epitaxial layer and the substrate.

19 ~~51~~. (Once Amended) The trenched field effect transistor of claim **[6]** 1 wherein said doped heavy body is formed by a double implant of said dopant of the second conductivity type.

52. The trenched field effect transistor of claim 51 wherein said double implant comprises a first high energy implant to reach said second depth, and a second lower energy implant to extend the heavy body from said second depth to substantially a surface of the substrate.

C7

53. (New) The trenched field effect transistor of claim 8, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the relative depths of the deepest portion of the heavy body and a depth of the well are controlled to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

54. (New) The trenched field effect transistor of claim 18, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the relative depths of a deepest portion of the heavy body and the depth of the well are controlled to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

~~55. (New) The trenched field effect transistor of claim 47, further comprising:~~

~~an epitaxial layer having the first conductivity type formed between the substrate and the well,~~

~~wherein the second depth and a depth of the well are controlled to eliminate the need for any layers disposed between the epitaxial layer and the substrate.~~

REMARKS

Upon entry of this amendment, which amends claims 1, 6-8, 10, 18, 47 and 50-51, cancels claim 13, and adds new claims 53-55, claims 1, 2, 5-12, 14-22 and 47-55 remain pending. Previously examined claims 1, 2, 5-22 and 47-52 were rejected under 35 U.S.C. 103(a) as being either anticipated by USPN 5,629,543 to Hshieh et al. (hereinafter Hshieh) or as being unpatentable over Hshieh in view of USPN 5,430,324 to Bencuya (hereinafter Bencuya) or USPN 5,783,491 to Nakamura et al. (hereinafter Nakamura). Reconsideration of the claims in view of the above amendments and the comments below is respectfully requested prior to examination of the CPA.

The Present Invention

The present invention is directed at a trench DMOS transistor that employs an "abrupt junction" at the interface between a heavy body disposed in a well of the transistor. This abrupt junction is laterally spaced away from the vicinity of the transistor's trench(es) and can be formed by, for example, performing a "double doping process" as described in detail on pages 11-12 of the application.

> "[I]t is preferred that the junction at the interface between the p- well and the p heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15, and a second boron implant at an energy of 30 to 40 keV and a dose of 1E14 to 1E15. The high energy first implant bring the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact 18."

One important characteristic of the "abrupt junction" aspect of the present invention is the predetermined and controlled depth of the junction. As described on page 12 of the application,

> "The resulting p+ heavy body junction is preferably about 0.4 to 1 µm deep…(final junction depth *after drive-in* is preferably about 0.5 to 1.5 µm deep."

The unique concentration profile of the p+ heavy body with respect to the p- well is depicted graphically in Fig. 5. Notice that the peak p+ heavy body is at a predetermined depth in the p-well and changes rapidly in a short further depth (i.e. has a steep doping concentration gradient) to form the abrupt transition with the p- well.

The abrupt junction in conjunction with the controlled positioning of its depth within the p- well is used to force the location of breakdown initiation away from the vicinity of the transistor's trench(es) and into the semiconductor. These aspects of the invention are unambiguously recited in independent claims 1, 8 and 47 of the application. For example, claim 1 recites that:

> "the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is controlled so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor."

Independent claims 8 and 47 each include a similar recitation.

Prior Art

Hshieh discloses a trenched DMOS transistor, which includes a "buried layer 16" having an "optimized doping profile." Hshieh teaches that the purpose of incorporating this "buried layer" is to "ensure that avalanche breakdown occurs at the buried layer/body region or buried layer/body contact region." (Col. 2, lines 8-10).

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Prior Art Distinguished

The foregoing summaries of both the present invention and Hshieh reveal that a common problem addressed by both relates to moving the point of breakdown initiation away from the vicinity of the transistor's trench(es). As explained below, however, Hshieh teaches a substantially different and inferior method and structure for addressing this problem.

The inventors of the present invention have proposed optimizing the p+ heavy body/p- well doping profile in the form of an "abrupt junction" that is positioned at a controlled depth within the well. Applicants would like to stress that Hshieh not only does not contemplate this proposed solution but in fact teaches away from it. Hshieh proposes a solution of inserting a "buried layer" having an "optimized doping profile" between the drain region (substrate 10) and the drift region (epitaxial layer 14) of the transistor.

Hshieh does disclose that the "body region 18" of the transistor described therein have "a doping concentration of e.g. $5x10^{16}/cm^3$" and a "p+ body contact region 24" having "a doping level of e.g. $10^{19}/cm^3$." However, one of skill in the art would not be able to ascertain, from these concentrations alone, what type of junction is formed between the two regions. Above, it was described how a double-implant technique is administered in one embodiment of the present invention to form an abrupt junction. There are other techniques that can be employed to form an abrupt junction. For example, one or a combination of the following can be used to form an abrupt junction: (1) using a high-energy implant (e.g. like the first implant of the double-diffused technique), (2) forming a shallow junction (e.g. by using a low diffusivity dopant), and (3) using a constant doping source. There is not even a remote suggestion by Hshieh to employ any one of these techniques, or anything similar thereto.

Besides failing to teach that the p+ body contact region/body region junction is abrupt, it should be emphasized that there is nothing in Hshieh that teaches or suggests that the junction between these two regions is of a controlled depth for the purpose of localizing the point of breakdown initiation within the device.

The very fact that Hshieh necessitates employment of a "buried layer" to control the breakdown initiation point shows that Hshieh does not teach, suggest or contemplate the present invention's claim of an abrupt junction having a predetermined and controlled depth within the p- well. If Hsieh it were obvious to use of an abrupt junction, Hshieh surely would not have included the buried layer. This is true since the use of a buried layer as taught by Hshieh has certain drawbacks not present in the present invention. First, not having to rely on a buried layer is beneficial, since it reduces the number of processing steps required in the overall fabrication process. Second, not requiring a buried layer eliminates the need to pay special attention to alignment of the buried layer relative to the deep body region during processing. Third, it allows the fabrication of higher density trench DMOS transistors, since the absence of the buried layer and the maintenance of the heavy body within the well corresponds to an elimination of obstructions – obstructions which would otherwise prevent a reduction in trench-to-trench pitch. It should be pointed out that Hshieh expressly recognizes the limitations on realizable device densities due to the presence of the buried layer. Specifically, in lines 34-35 of column 3, Hshieh explains that in order to increase device density, "the goal is" to form "as narrow a buried layer region as possible." In fact, as best understood by Applicants, the use of a buried layer as taught by Hshieh may indeed exacerbate the breakdown problem at reduced pitch because it may bilaterally diffuse too close to corners of the trench(es).

Finally, Applicants wish to report that incorporation of some or all of the embodiments of the present invention into various of Applicant's products (e.g. the Fairchild Semiconductor FDS 6680A, FDS 6612A and FDS 6690A power transistor products, to name a few) has led to substantial commercial success. Other competitors have attempted to solve the breakdown problem by other means yet have failed. Therefore, the commercial success of Applicant's products, which incorporate embodiments of the present invention further supports the assertion that the present invention is not obvious.

Based on the foregoing, Applicants respectfully believe that Hshieh cannot be maintained as a §102(e) and 103(a) reference against claims 1, 8 and 47. Neither Bencuya nor

Nakamura add anything to change this assertion. For these reasons, Applicants respectfully request that the rejections of these claims be withdrawn.

Claims 2, 5-7, 50-52 depend from claim 1; claims 9-17, 46 and 53 depend from claim 8; and claims 48-49 and 55 depend from claim 47. Because these dependent claims all depend from what Applicants believe to be allowable base claims, they too should be in condition for allowance. However, these dependent claims incorporate additional novel features of their own, which are not taught or suggested by any of the cited references. For example, claim 7 recites that the "heavy body has a first dopant concentration near the abrupt junction and a second dopant concentration near its upper surface that is less than the first dopant concentration." The cited references fail to teach or suggest this aspect of the present invention. Another example relates to claims 50, 53 and 54. Each of these claims recite that the trenched field effect transistor claimed in claims 1, 8 and 18, respectively, further comprise an "epitaxial layer…formed between the substrate and the well." These claims also recite how the relative depths of the heavy body and well are controlled "to eliminate the need for any additional layers between the epitaxial layer and the substrate." None of the cited references teach or suggest this aspect of the invention either.

The remaining independent claim, claim 18, is also distinguishable over the prior art. As described above, claim 18 includes a "field termination structure" that is "in contact with the heavy body surrounding the periphery of the [cell] array" and extends "into the semiconductor substrate to a depth that is deeper than said depth of said well." Applicants have found no teaching or suggestion of the termination structure of the type claimed in the cited references. Despite this, the Examiner rejected claim 18 in the February 7, 2000 Office Action solely on the basis that "Claims reciting field termination structure are obvious." Applicants respectfully disagree with the Examiner's examination and assessment of claim 18, particularly since the Examiner has not provided any reason(s) for the rejection, as is required by MPEP § 2142. Accordingly, Applicants respectfully request that the Examiner either provide a basis for the rejection of claim 18 or withdraw the rejection. Claims 19-21 and 54

depend from claim 18. Because these dependent claims depend from an allowable base claim, they too should be in a condition for allowance.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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